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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,225	06/09/2000	David Robert Baldwin	TD-155	3467

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EXAMINER	
TUNG, KEE M	
ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,225	BALDWIN, DAVID ROBERT	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-10 and 12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10 and 12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed 9/20/05 has been considered in preparing this Office action.

Note: The claim status of the newly added claims 21 and 22 should be –New— not "currently proposed".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-10 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meinerth et al (6,124,865 hereinafter "Meinerth") in view of Jim Blinn (The truth About Texture Mapping).

Meinerth teaches a computer system (Figs. 1, 2A and 2B) comprising a graphics accelerator unit (graphics processing unit 210) which can transfer data (not particularly suggest that the data is **texture data** for the graphics processing unit and the transfer of data is when/after the **page fault** is occurred) from main memory (140) to frame buffer (164) including virtual memory, without any action by the host processor (abstract; col. 5, lines 44-49 and col. 6, lines 21-25). However, it is old and well known in the art that texture mapping is considered one of the many functions performing by 3D graphics accelerator in order to provide realistic representation of the object in 3D space.

Meinerth further teaches the video device 161 may be a 3D video device or graphics accelerator (Fig. 9 and col. 19, lines 3-5). Blinn teaches page fault occurs when accessing texture data from memory fails and the data is transfer from another storage device into the memory (page 79, col. 1 at the bottom). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teaching of Blinn into the system of Meinerth in order to add realism to the computer generated graphic in the 3D space. Therefore, at least claim 1 would have been obvious.

Claim 2 is similar in scope to claim 1, Meinerth additionally teaches the host processor transfers texture data when said graphics accelerator unit calls for data which has not been recently been present in said main memory (col. 9, lines 39-55).

Claim 3 is similar in scope to claim 1, Meinerth further teaches at least one CPU (106), operatively connected to have read/write access to a main memory (140); first memory management logic (col. 9, lines 39-55, and is also inherent to any well known computer system to include MMU to manage virtual memory by using translation unit 108 and Blinn, page 79, under Virtual Memory), which virtualizes said main memory with reference to at least one bulk storage unit (such, as, disk memory 191); a graphics accelerator unit (210), comprising rendering accelerator logic (210), dedicated graphics memory (164), and a second memory management unit (Fig. 3, 154 and inherent by the teachings of virtual translation unit 230 under "virtual Translation" from col. 7, line 1 to col. 11, line 57) which manages texture data for said accelerator logic and performs page faulting (Blinn, page 79, col. 1) of said texture data, invisibly to the host processor

(col. 5, lines 44-49 and col. 6, lines 21-25). Therefore, at least claims 3 and 13 would have been obvious.

Claim 4 is similar in scope to claim 3, Meinerth further teaches a host processor (CPU 106) having host physical memory (main memory 140) associated therewith, and a graphics accelerator unit (210) having respective local memory (164) associated therewith; wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data **automatically** (without any action by CPU; col. 5, lines 44-49 and col. 6, lines 21-25) and the graphics accelerator unit also having a graphics memory manager (Fig. 3, 154 and inherent by the teachings of virtual translation unit 230).

As per claim 5, Meinerth teaches after fetching said texture data, said graphics memory manager restarts texture processing (col. 9, lines 46-55, such as, restart the graphics system).

Claim 7 is similar in scope to claim 3, Meinerth further teaches having virtual memory management (col. 9, lines 39-55, and is also inherent to any well known computer system to include MMU to manage virtual memory by using translation unit 108 and Blinn, page 79, under Virtual Memory); and a graphics accelerator unit also having a virtual memory management (Fig. 3, 154 and inherent by the teachings of virtual translation unit 230 under "virtual Translation" from col. 7, line 1 to col. 11, line 57); and wherein, when said graphics accelerator unit attempts to access texture data which is in said host physical memory, if said texture data is in said host physical

memory, said graphics memory manager fetches said texture data therefrom automatically (without any action by CPU; col. 5, lines 44-49 and col. 6, lines 21-25); and if said texture data is not in said host physical memory, said texture data is first loaded into said host physical memory, and thereafter said graphics memory manager fetches said texture data automatically from said host physical memory (col. 9, lines 39-55). Therefore, at least claim 7 would have been obvious.

As per claim 8, Meinerth teaches said graphics accelerator unit also includes a PCI/AGP interface (would have been obvious to one of ordinary skill in the art to replace bus 169 by an AGP bus interface in order to provide fast access to the main memory by the graphics processing unit), DMA controller (not shown, but would have been obvious by the teachings of direct data transfer between main memory and frame buffer, col. 6, lines 64-67; by definition, DMA provides directly data transfer between main memory and other device, such as, frame buffer, without involve the host CPU), SGRAM/SDRAM (would have been obvious to one of ordinary skill in the art to replace the video RAM of frame buffer 164 by other type of memory, such as, SGRAM/SDRAM without any burden), a RAMDAC (166), and a video stream interface (such can be interface to/from network bus 180 and I/O device 192).

As per claim 9, Meinerth teaches said dedicated graphics memory is SGRAM/SDRAM to which the unit has read/write access through its frame buffer and local buffer ports (obvious in view of the frame buffer 164 to replace by SGRAM/SDRAM type memory).

As per claims 10, 16 and 19, Meinerth teaches said host processor (106) is operatively connected to receive inputs from input devices (192) through an interface manager chip (220) which provides an interface various ports and registers.

As per claim 12, Meinerth fail to explicitly suggest or teach said first memory management logic is a bridge controller (220). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to modify the teachings of memory control unit 220 of Meinerth to include the memory management logic because in order to manage or control the access of the main memory in efficient and effective manner. Therefore, at least claim 12 would have been obvious.

Claim 14 is similar in scope to the combination of claims 3 and 8, and thus is rejected under similar rationale.

Claim 15 is similar in scope to claim 3, and additionally requires the second memory management unit (see under "virtual Translation" from col. 7, line 1 to col. 11, line 57) also manages texture storage in the main memory in addition to managing texture storage in normal texture memory (such as, texture memory in Blinn, page 79, col. 2, top or frame buffer of Meinerth because some stores texture data in frame buffer).

Claim 17 is similar in scope to the combination of claims 4 and 8, and thus is rejected under similar rationale.

Claim 20 is similar in scope to the combination of claims 7 and 8, and thus is rejected under similar rationale.

As per claim 21, the combined system teaches where the page is located in the host memory to be manipulated is located (not explicitly suggest, but would have been obvious to Meinerth in order to properly retrieve the data from the main memory to frame buffer either by the memory address location or from the translation table or unit, col. 5, lines 44-49, col. 6, lines 21-25 and col. 9, lines 39-55); and wherein said accelerator unit determines which page out of the working set to be use, marks this page the most recently used page (Blinn, page 79, col. 1 at the bottom), and updates the page tables for the new page and remove any reference to the page just bumped out of memory (col. 9, lines 39-55).

Claim 22 is similar in scope to the combination of claims 3 and 21, and thus is rejected under similar rationale.

Response to Arguments

3. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671